AP-IL CHIP

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	AS ISSUED	11-27-79	

Model No.	Stock No. 1LB6-4001
Title 1LB6 (PIL)	
Description ELECTRICAL SPECIFICATION	Date 11-27-79
By CARL LANDSNESS	Sheet No. 1 of 14
Supersedes	Drawing No. A-1LB6-4001-1

I. ABSOLUTE MAXIMUM RATINGS:

1.1 SUPPLY VOLTAGE V_{CC} (GND = V) ..... +10 VOLTS
1.2 STORAGE TEMPERATURE ..... -50°C to +150°C
1.3 OPERATING TEMPERATURE ..... 0°C to 65°C
1.4 HUMIDITY ..... 0 to 90%
1.5 VOLTAGE AT ANY INPUT OR OUTPUT PIN ..... GND -0.3V to V_{CC} +0.3V
1.6 INPUT TRANSIENT PROTECTION STANDARD ..... 500 VOLTS (SEE FIG. 1)
1.7 INPUT TRANSIENT PROTECTION ON RXDO,RXD1,TXDO,TXD1.... 5000 VOLTS

II. OPERATING CONDITIONS: $0°C \leq T_A \leq 45°C$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENTS
GND	GROUND	0.0	0.0	0.0	V	
V_{CC}	SUPPLY VOLTAGE (SUBSTRATE)	6.0	6.25	7.0	V	
ICCOP	V_{CC} OPERATING CURRENT			2.5	mA	V_{CC}=6.5V OUTPUT LOADS=MAX. FREQ.=MAX RXDO,RXD1,$\overline{SCTL}$=0
ICCST	V_{CC} STANDBY CURRENT			1.0	uA	V_{CC}=5.0V, GND=0V ISA, DATA, RXDØ, RXD1, Ø1, Ø2. SYI PWO=0V. All othe pins open.
ICCTR	V_{CC} OPERATING CURRENT WHILE RETRANSMITTING			3.5	mA	V_{CC}=6.5V FREQ.=M 1.6K LOAD BETWE TXDO, TXD1; Out- put loads=max; Frame retransmit every other fram time.
INPUT PARAMETERS:						
VIH	INPUT LOGIC "1" VOLTAGE LEVEL	V_{CC} -1.25	.8V_{CC}		V	All inputs excep RXDØ, RXD1
VIL	INPUT LOGIC "0" VOLTAGE LEVEL		.2V_{CC}	GND+1.25	V	

LTR	P.C. NO	APPROVED	DATE	REVISIONS

MODEL | STK NO 1LB6-4001

1LB6 ELECTRICAL SPECIFICATION

BY CARL LANDSNESS | DATE 11-27-79

APPD | SHEET NO 2 OF 14

SUPERSEDES | DWG NO A-1LB6-4001-1

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENTS
VRXH	INPUT LOGIC "1" ON RXDO, RXD1	4.2			V	PIL FREQ=MIN.
VRXL	INPUT LOGIC "0" ON RXDO, RXD1			GND+1.25V	V	PIL FREQ=MIN. TRPW=MIN.
VRXTH+	HIGH LEVEL THRESHOLD ON RXDO, RXD1	2.2	3.3	4.2	V	
VRXTH-	LOW LEVEL THRESHOLD ON RXDO, RXD1	1.25	2.3	3.3	V	
VRXHYS	INPUT HYSTERISIS ON RXDO, RXD1	0.5V			V	
ILIN	INPUT LEAKAGE CURRENT ON INPUT PINS			0.1	uA	AT 6.5V to GND AND V_{CC}, EXCEPT TSTCLK, $\overline{SCTL}$
ILIO	INPUT LEAKAGE CURRENT ON I/O PINS			1.0	uA	AT 6.5V to GND V_{CC}. PINS TRI-STATED EXCEPT LC
	INPUT CURRENT					LC2 V_{CC}=6.5V V_{CC}=6.5V
IHTCLK	TSTCLK HIGH CURRENT			+50	nA	AT 6.5V
ILTCLK	TSTCLK LOW CURRENT	-0.15		-0.01	mA	AT ØV
IHSCTL	$\overline{SCTL}$ HIGH CURRENT	0.05		+0.5	mA	AT 6.5V
ILSCTL	$\overline{SCTL}$ LOW CURRENT	-50			nA	AT ØV
CIN	INPUT CAPACI-TANCE			8	pF	ALL INPUT AND I/ PINS
	OUTPUT PARAMETERS:					
VOH	OUTPUT LOGIC "1" VOLTAGE LEVEL	V_{CC} -1.0	Ø.83V_{CC}		V	ALL OUTPUTS EXCE LC1, LC2

LTR	P C NO	APPROVED	DATE	REVISIONS

MODEL | STK NO 1LB6-4001

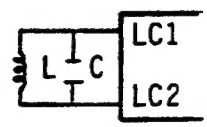
1LB6 ELECTRICAL SPECIFICATION

BY CARL LANDSNESS | DATE 11-27-79

APPD | SHEET NO 3 OF 14

SUPERSEDES | DWG NO A-1LB6-4001-1

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENTS
VOL	OUTPUT LOGIC "0" VOLTAGE LEVEL		Ø.17V_{CC}	GND+1.0	V	ALL OUTPUTS EXCEP LC1, LC2
COUT	OUTPUT CAPACITANCE DRIVE CAPABILITY					THESE OUTPUTS WIL DRIVE THE SPECIF CAPACITANCE BE- TWEEN VOL AND VOH WITHIN TDV. (SEE FIG. 2 & 4)
	DATA	200			pF	
	FLGIN	150			pF	
OUTPUT CURRENT (DC)						V_{CC}=MIN.
IHISA	ISA HIGH SOURCE CURRENT	0.5			mA	AT V_{OH}
ILFIN	FLGIN LOW SINK CURRENT			-0.35	mA	AT V_{OL}
IHTXD	TXDO,TXD1 HIGH SOURCE CURRENT	8.5		65.0	mA	AT V_{CC} -0.5V
ILTXD	TXDO,TXD1,LOW SINK CURRENT	-65.0		-8.5	mA	AT 0.5V
41C TIMING PARAMETERS:						
TP	CLOCK PERIOD	2.63	2.78	2.95	uS	SEE FIG. 2
TPW1	Ø1 PULSE WIDTH	500	2/8 of TP	750	nS	SEE FIG. 2
TPW2	Ø2 PULSE WIDTH	500	2/8 of TP	750	nS	SEE FIG. 2
TCD	Ø1 to Ø2 DELAY	900	3/8 of TP	1200	ns	SEE FIG. 2
TR, TF	CLOCK RISE, FALL TIME		50		nS	SEE FIG. 2

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENT
TDV	OUTPUT DATA VALID		3/8 of TP	1000	nS	AFTER TRAILING EDGE OF Ø2. SEE FIG.2 FOR ALL LIN EXCEPT ISA AT A ZERO LEVEL AND DA AT EITHER LEVEL.
			3/8 of TP	800	nS	FOR ISA AT A ZERO LEVEL AND DATA AT EITHER LEVEL.
TSU	INPUT DATA SETUP TIME	550	2/8 of TP		nS	BEFORE TRAILING EDGE OF Ø1. SEE FIG. 2. ISA,DATA, SYNC,PWO INPUTS.
PIL TIMING PARAMETERS:						
THE FOLLOWING TIMING SPECIFICATIONS ARE FOR L AND C AS SHOWN.						
C	CAPACITANCE	114.0	120	126.0	pF	
L	INDUCTANCE	53.2	56	58.8	uH	
R_L	INDUCTOR SERIES RESISTANCE			6	Ω	
TLC	OSCILLATOR PERIOD	475	500	550	nS	MEASURED AT LC1 AND LC2 (MEASURIN PROBE C<1pF)
TCLK	TSTCLK INPUT PERIOD	450	500	550	nS	
TCLKR TCLKF	TSTCLK RISE & FALL TIME		50		nS	
TRXPW	RXDO,RXD1 PULSE WIDTH	650		1.5	ns	SEE FIG.4
TRXTR	RXDØ,RXD1 TRANSITION TIME			300	nS	
TRXSU	RXDO,RXD1 SETUP TIME	50			nS	BEFORE TRAILING EDGE OF TCLK. SEE FIG.4

LTR	P C NO	APPROVED	D
REVISIONS			

MODEL | STK NO 1LB6-4001

1LB6 ELECTRICAL SPECIFICATION

BY CARL LANDSNESS | DATE 11-27-79

APPD | SHEET NO 5 OF 14

SUPERSEDES | DWG NO A-1LB6-4001-1

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENT
TRXHD	RXDO,RXD1 HOLD TIME	50			nS	AFTER TRAILING EDGE OF TCLK. SEE FIG.4
TRXLO	RXDO,RXD1 LOW TIME BETWEEN PULSES	1.3			uS	
TRXOV	RXDO,RXD1 OVER-LAP TIME	0		300	nS	
TTXPW	TXDO,TXD1 PULSE WIDTH	950	2xTLC OR 2xTCLK	1200	nS	MEASURED WITH 470pF LOAD. SEE FIG.5
TTXTR	TXDØ,TXD1 TRANSITION TIME			120	nS	MEASURED WITH 470pF LOAD. SEE FIG.5
TTXOV	TXDØ,TXD1 OVERLAP TIME	0		120	nS	MEASURED WITH 470pF LOAD. SEE FIG.5

III. SUMMARY OF SIGNALS:

SIGNAL	I/O	DESCRIPTION
Ø1, Ø2	IN	41C SYSTEM CLOCKS
SYNC	IN	PROVIDES SYSTEM TIMING AND INDICATES THE PRESENCE OF A SYSTEM INSTRUCTION ON THE ISA LINE. WHEN PWO IS LOW, SYNC=DPWO.
DATA	I/O	USED TO TRANSFER 56 BIT SERIAL DATA (LSB FIRST) TO AND FROM CPU C REGISTER. DATA SOURCED FROM PIL ONLY DURING WORD TIMES FOLLOWING 2nd AND 3rd WORD TIMES OF A C=PIL INSTRUCTION (READ FROM PIL). TRI-STATED AT ALL OTHER TIMES AND ALWAYS DURING Ø2.
ISA	I/O	USED TO RECEIVE ROM DATA (INSTRUCTIONS) AT T44-T53. ISA IS PULLED HIGH WHEN REQUESTING CPU TO WAKE UP FROM LIGHT SLEEP IN RESPONSE TO PIL FLAGS-IFCR+SRQR+FRNS+FRAV. TRI-STATED BY PIL WHEN PWO IS HIGH.
PWO	IN	HIGH WHEN IN RUN MODE. USED ALONG WITH SYNC FOR INITIALLIZING CIRCUITS.

SIGNAL	I/O	DESCRIPTION
FLGIN	OUT	PULLS LOW DURING FIRST 3 BIT TIMES AND PULLS HIGH DURING LAST BIT TIME OF DIGITS 6-10 IF PIL FLAGS ARE SET AND FLAGS ARE ENABLED (PROGRAMMABLE). OTHERWISE THIS LINE IS TRI-STATED. IT IS ALWAYS TRI-STATED DURING Ø2.
V_{CC}	IN	POSITIVE VOLTAGE SUPPLY (SUBSTRATE).
GND	IN	NEGATIVE VOLTAGE SUPPLY.
LC1, LC2	I/O	PINS FOR PARALLEL LC CONNECTION FOR PIL 2MHz OSCILLATOR. OSCILLATOR IS UNDER PROGRAM CONTROL..
TSTCLK	IN	ALLOWS EXTERNAL CLOCK TO BE FED TO CHIP IN LIEU OF 2 MHz OSCILLATOR. INTERNALLY PULLED HIGH. WHEN USED, LC2 MUST BE PULLED HIGH AND EXTERNAL LC DISCONNECTED.
RXDØ,RXD1	IN	RECEIVER INPUTS FROM RECEIVER TRANSFORMERS. SCHMITT TRIGGER BUFERS ARE USED TO PROVIDE NOISE IMMUNITY.
TXDØ,TXD1	OUT	TRANSMITTER OUTPUTS TO DRIVER TRANSFORMERS.
$\overline{\text{SCTL}}$	IN	WHEN TIED LOW, CHIP WAKES UP AS SYSTEM CONTROLLER. INTERNALLY PULLED LOW.

IV. IC TEST CONDITIONS:

The preceeding pages show specifications for the 41C chips for an operating range of 0 to 45 degrees C. To insure proper operations at these temperatures, V_{CC} should be adjusted to compensate for room temperature testing as well as providing enough guard band on the part during wafer and package tests for both high and low V_{CC}.

OPER. PT. 1 MIN. V. MAX F	VCC=5.5V 41C FREQ=380K PIL FREQ=2.2M	VCC=5.5V 41C FREQ=380K PIL FREQ=2.2M	VCC=5.7V 41C FREQ=380K PIL FREQ=2.2M
OPER. PT. 2 MAX.V, MIN.F	VCC=7.2V 41C FREQ=340K PIL FREQ=1.8M	VCC=7.1V 41C FREQ=340K PIL FREQ=1.9M	VCC=7.0V 41C FREQ=340K PIL FREQ=1.8M

The above table shows the different test conditions for the wafer test

package test, and thepart spec. (QA) test. All test programs should do functional tests on the part for both operating points. The table below shows a detailed breakdown of recommended values for these operating points, and a general guide for DC parametric test guard banding.

PARA	WAFER	PKG	QA	WAFER	PKG	QA
	LOW VOLTAGE			HIGH VOLTAGE		
VHRX	4.1	4.1	4.2	4.1	4.1	4.2
VLRX	1.25	1.25	1.25	1.25	1.25	1.25
VCC	5.5	5.5	5.7	7.2	7.1	7.0
VIH	4.25	4.25	4.45	5.95	5.85	5.75
VIL	1.25	1.25	1.25	1.25	1.25	1.25
VOH	4.5	4.5	4.7	6.0	6.0	6.0
VOL	1.0	1.0	1.0	1.0	1.0	1.0
	HIGH FREQUENCY			LOW FREQUENCY		
TP	2630	2630	2630	2950	2950	2950
TPW1	500	500	500	750	750	750
TPW2	500	500	500	750	750	750
TCD	900	900	900	1200	1200	1200
TDV	1000	1000	1000	1000	1000	1000
TSU	550	550	550	550	550	550
TCLK	450	450	450	550	550	550
	DC PARAMETRIC			TEST CONDITIONS		
ICCOP	2.0	2.25	2.5	VCC=6.5V, FREQ=MAX		
ICCST	0.8uA	0.9uA	1uA	VCC=5.0V, STATIC		
ILIN	90nA	100nA	--	VCC=10V, VIN=GND and VCC		
ILIO	.8uA	.9uA	1uA	VCC=6.5V, VIN=GND and VCC		
ICCTR	2.8	3.15	3.5mA	VCC=6.5V FREQ=MAX		

PARA	WAFER	PKG	QA	WAFER	PKG	QA
	DC PARAMETRIC			TEST CONDITIONS		
ILTCLK	-120uA	-135uA	-150uA	@ØV		
IHSCTL	400uA	450uA	500uA	@6.5V		
IHISA	500uA	500	500uA	@VOH @VCC (MIN)		
ILFIN	-350uA	-350	-350uA	@VOL @VCC (MIN)		
IHTXD (MIN)	9.0mA	8.7mA	8.5mA	@VCC -0.5V		
ILTXD (MAX)	-9.0mA	-8.7mA	-8.5mA	@0.5V		
IHTXD (MAX)	60mA	62mA	65mA	@VCC-0.5V		
ILTXD (MIN)	-60mA	-62mA	-65mA	@0.5V		
	STRESS TEST			COMMENTS		
VSTRESS	10V	---	---	OPERATE PARTS AT MAX. FREQ. WITH VCC= VSTRESS FPR 1 LMLOAD. IGNORE FAILURES.		

LTR	P.C. NO	APPROVED	REVISIONS

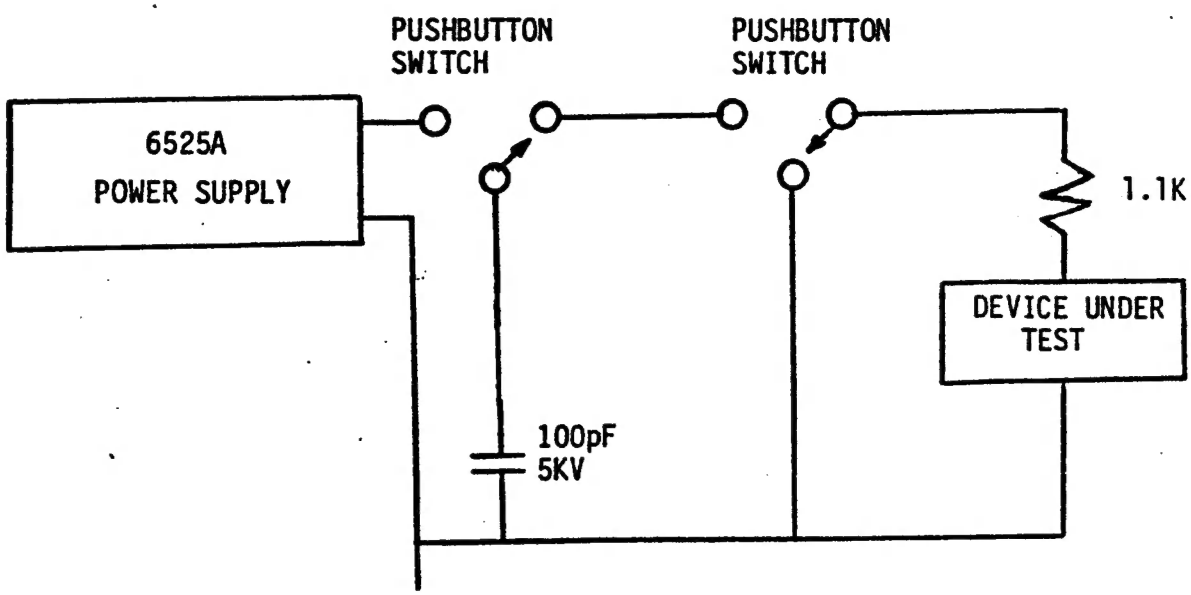
MODEL | STK NO 1LB6-4001

1LB6 ELECTRICAL SPECIFICATION

BY CARL LANDSNESS | DATE 11-27-79

APPD | SHEET NO 9 OF 14

DWG NO A-1LB6-4001-1



GATE PROTECTION TEST CIRCUIT

FIGURE 1

LTR	P C NO	APPD	DATE
		REVISIONS	

MODEL | STK NO 1LB6-4001

1LB6 ELECTRICAL SPECIFICATION

BY CARL LANDSNESS | DATE 11-27-79

APPD | SHEET NO 10 OF 14

SUPERSEDES | DWG NO A-1LB6-4001-1

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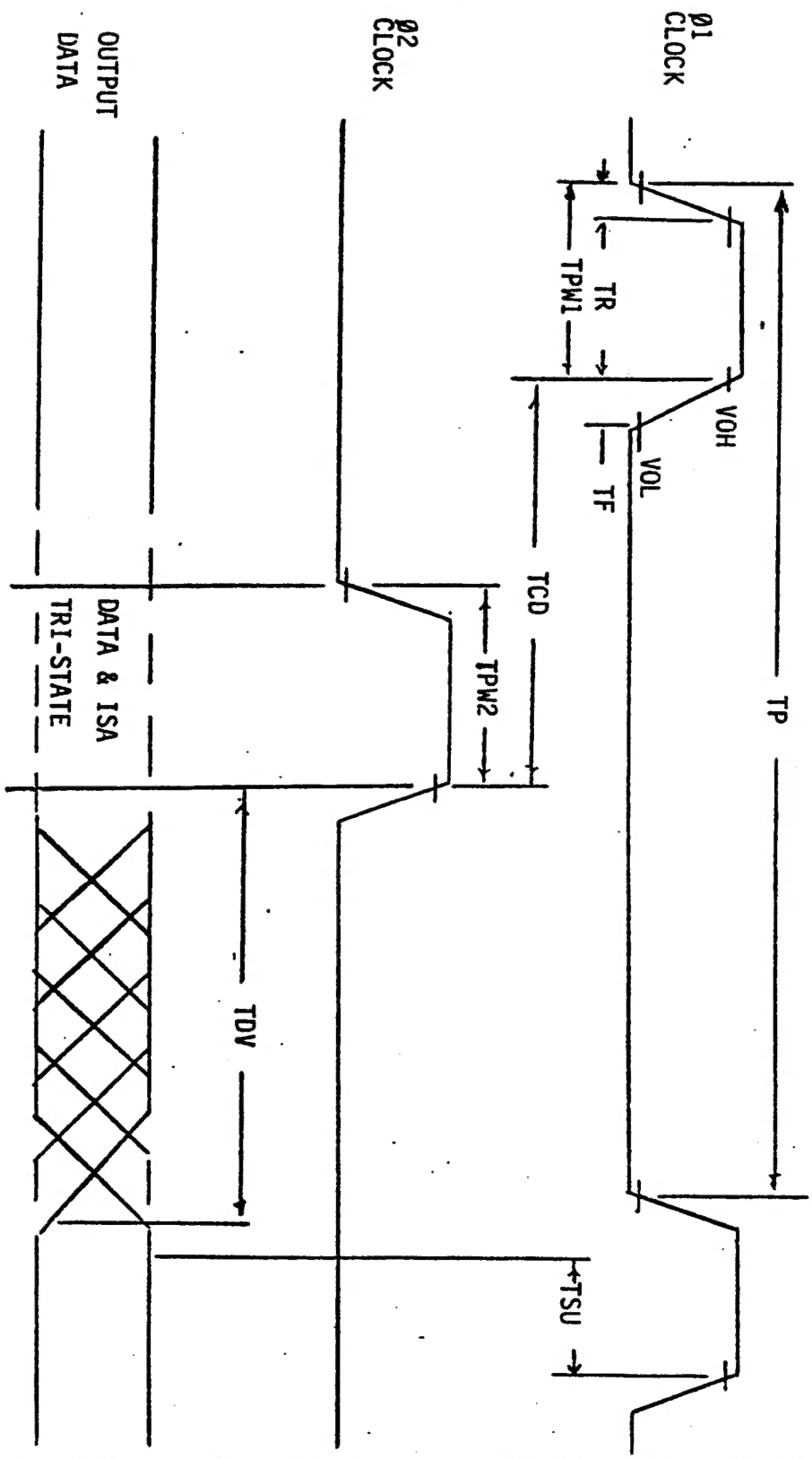


NUT SYSTEM CLOCK WAVEFORMS (FIGURE 2)

LTR	P C NO	APPROVED	DATE	REVISIONS

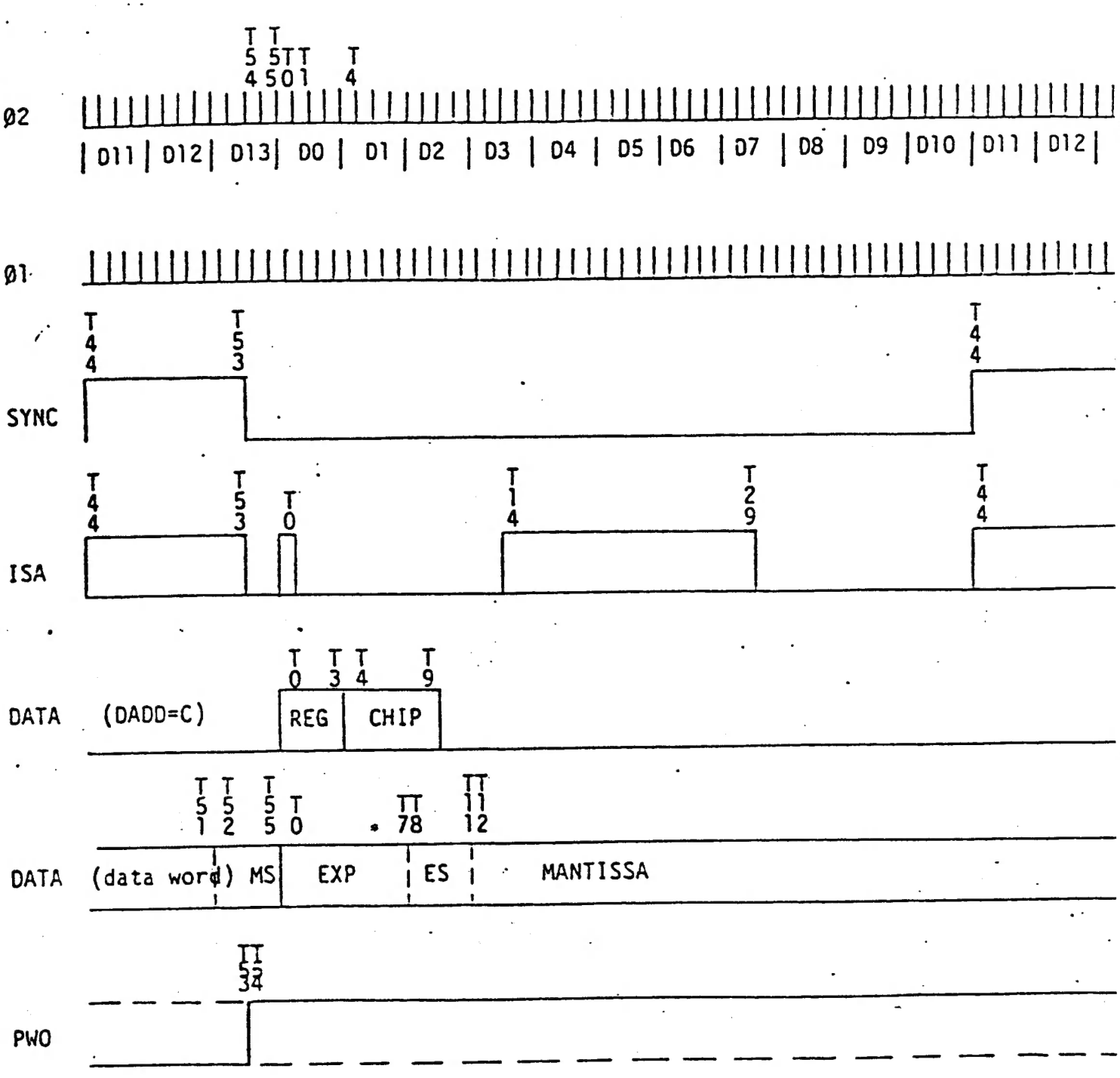
MODEL | STK NO 1LB6-4001

1LB6 ELECTRICAL SPECIFICATION

BY CARL LANDSNESS | DATE 11-27-79

APPD | SHEET NO 11 OF 14

DWG NO A-1LB6-4001-1



NUT SYSTEM TIMING

(Figure 3)

	SEE	SHEET 1		MODEL	STK NO 1LB6-4001
				1LB6 ELECTRICAL SPECIFICATIONS	
				BY CARL LANDSNESS	DATE 11-27-79
				APPD	SHEET NO 12 OF 14
LTR	P C NO	APPROVED	TE		

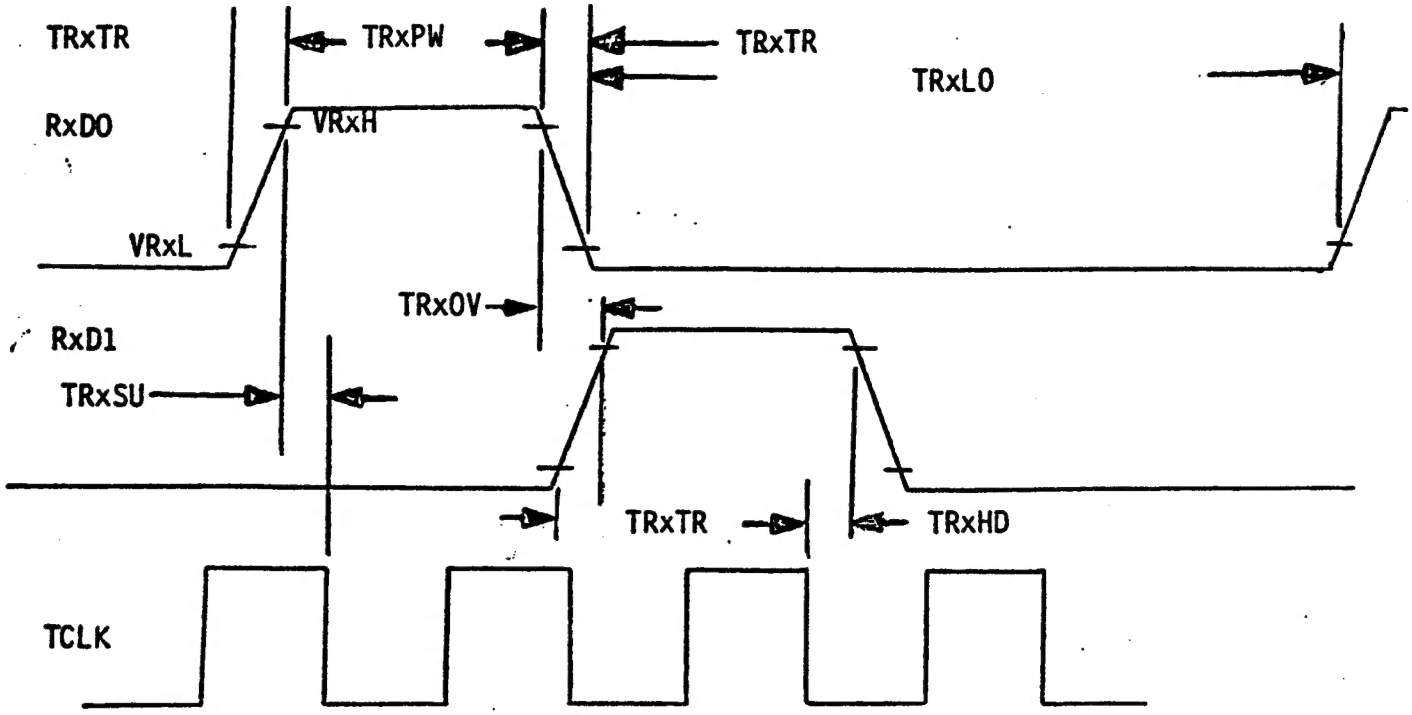


FIGURE 4 - PIL RECEIVER TIMING

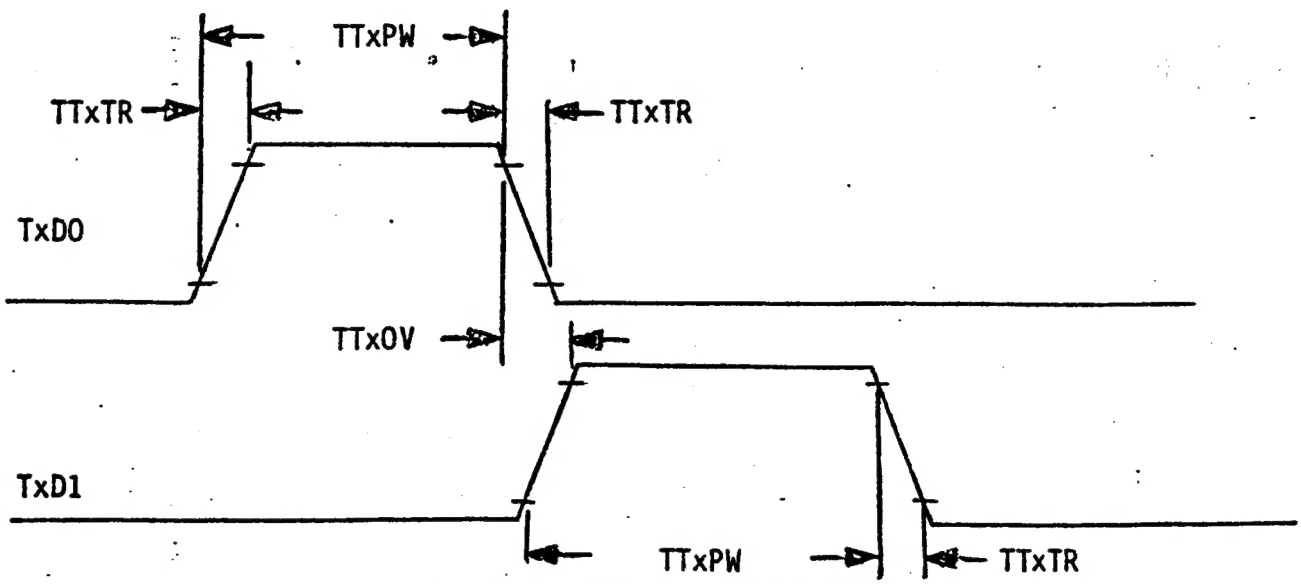
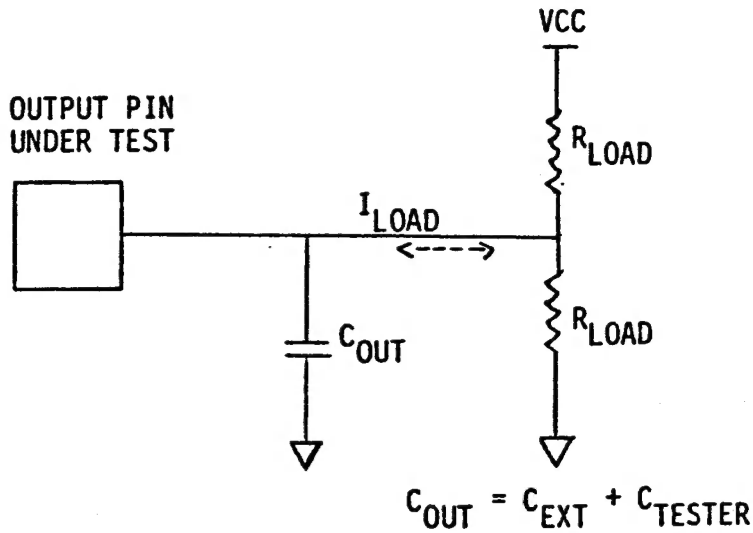


FIGURE 5 - PIL TRANSMITTER TIMING

LTR	P.C. NO	APPROVED	DATE
	REVISIONS		

MODEL	STK NO 1LB6-4001
1LB6 ELECTRICAL SPECIFICATION	
BY CARL LANDSNESS	DATE 11-27-79
APPD	SHEET NO 13 OF 14
SUPERSEDES	DWG NO A-1LB6-4001-1



TEST CONDITION FOR OUTPUT PINS
(Figure 4)

I_{LOAD} for specified C_{out} is 0. For testers with I_{LOAD} 0, modify C_{OUT} to C_{NEW} with the following formulas to compensate for the load. Also I_{LOAD} should maintain an equal sinking and sourcing level to make the modification valid.

$$I_{AVE} = C \frac{dV}{dT}$$ Basic formula

$$I_{AVE} = C_{OUT} \times \frac{VOH - VOL}{TDV}$$ Normal device drive

$$I_{LOAD} = C_{MOD} \times \frac{VOH - VOL}{TDV}$$ Calculate C_{MOD} for extra load current required for the device.

$$C_{NEW} = C_{OUT} - C_{MOD}$$

$$C_{NEW} = C_{OUT} - \frac{I_{LOAD} \times TDV}{VOH - VOL}$$ Modification formula

	SEE	SHEET 1		MODEL	STK NO 1LB6-4001
				1LB6 ELECTRICAL SPECIFICATIONS	
				BY CARL LANDSNESS	DATE 11-27-79
				APPD	SHEET NO 14 OF 14
LTR	P C NO	APP	DATE	SUPERSEDES	DWG NO A-1LB6-4001-1
		REVISIONS			